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A Comparative Study of CMOS and Carbon Nanotube Field Effect Transistor Based Inverter at 32 nm Technology Node†

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Carbon nanotube field effect transistor is emerging as new promising device for future nanotechnology solutions. It utilizes semiconducting carbon nanotube as its channel whose quasi 1-D structure provides high mobility for near ballistic transport and better electrostatic control. In this paper we have designed a basic inverter circuit using carbon nanotube field effect transistor. The key performances of inverter such as noise margin, average power and delay time are analyzed and compared with CMOS inverter. Both the inverters are simulated in HSPICE platform. The simulated results of carbon nanotube field effect transistor inverter shows improved performance in terms of noise margin, power and delay time than CMOS inverter.

Key Words: CMOS, Carbon nanotube field effect transistor, Inverter, Noise margin, Power dissipation, Delay.

INTRODUCTION

Silicon based technology has experienced a large growth in the last few decades. Scaling of the metal oxide semiconductor field effect transistor devices to increasingly smaller dimensions leads to certain degradations in performances. Significant increase in short channel effects including threshold voltage roll off, drain induced barrier lowering and leakage currents including weak inversion current, drain induced barrier lowering current and reverse *p-n* junction current are introduced by the scaling of the device. Thus it causes degradation in terms of power and performance at the system level. So semiconductor industry is trying to overcome the limitations of traditional silicon metal oxide semiconductor field effect transistors by integrating new promising nano scaled devices with silicon based technology. The carbon nanotube field effect transistor (CNFET) is emerging as one of the alternatives where semiconducting carbon nanotube is used as the channel. Its quasi 1-dimensional (1-D) structure provides better electrostatic control over the channel region than 3-dimensional (3-D) device like bulk CMOS. It provides high drive current due to larger current carrier mobility, high transconductance with low power consumption and low noise. Carbon nanotubes are long thin cylinders of carbon first discovered by Ijima in Japan in the year 1991[1]. These consist of hexagonal lattice of carbon layers that are folded in the form of cylinders.

Fig. 1 shows the simple cross sectional drawing of carbon nanotube field effect transistor with some key structural parameters. L_{ch} denotes the length of the channel; Pitch is the distance between the centers of two adjacent carbon nanotubes within the same device. W_{gate} denotes the width of the metal gate and T_{ox} denotes the thickness of gate oxide layer. Once the nanotube is grown its diameter cannot be adjusted anymore. So to increase the width of the transistor to get greater driving current capability, a number of parallel tubes are grown[2].

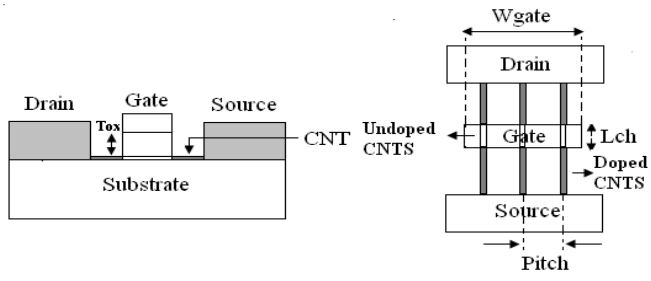

Fig. 1. Structure of CNFET

In terms of device operation mechanism, carbon nanotube field effect transistors are classified as either Schottky barrier controlled (SB) FETs or metal oxide semiconductor like FET[3]. However, the ambipolar behaviour of SB-carbon nanotube field effect transistor makes it undesirable for complementary logic design. It also suffers from poor AC performance due to prox-

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imity of gate electrode to S/D metal. So considering both the fabrication feasibility and superior device performance of metal oxide semiconductor field effect transistor like carbon nanotube field effect transistor compared to SB-carbon nanotube field effect transistor, we have focused on metal oxide semiconductor field effect transistor like carbon nanotube field effect transistor. Predictive technology model and stanford university model has been used here for the simulation of CMOS and carbon nanotube field effect transistor based inverter circuit respectively at 32 nm technology node[4,5].

CIRCUIT LEVEL IMPLEMENTATION

For comparing the performance of carbon nanotube field effect transistor with CMOS at circuit level the inverter as a fundamental logic gate is considered here. The voltage transfer characteristics (VTC) of carbon nanotube field effect transistor inverter is compared with that of CMOS inverter. The power supply voltage (V_{dd}) used here is 0.9 V and channel length considered is 32 nm. For designing CMOS inverter, a ratio of 3 (PMOS:NMOS) is used to obtain a symmetrical shape at $V_{dd}/2$ in 32 nm technology. Since the driving capability of *n*-carbon nanotube field effect transistor is almost similar to *p*-carbon nanotube field effect transistor, a ratio of 1:1 (*p*-CNFET: *n*-CNFET) is used to obtain the symmetrical shape. The diameter of the each carbon nanotube is chosen to be 1.5 nm. Pitch between each parallel nanotube is taken as 20 nm and W_{gate} is chosen to be 120 nm where maximum number of nanotubes utilized for simulation is 6. Thicknesss of the oxide layer is 4 nm.

RESULTS AND DISCUSSION

The voltage transfer characteristics of carbon nanotube field effect transistor inverter and CMOS inverter for 0.9V and applying different power supplies is shown in Fig. 2(a) and Fig. 2(b) respectively. The voltage transfer characteristics of carbon nanotube field effect transistor inverter shows a steeper curve in the transition region due to higher gain. From Fig. 2(a) the values of the V_{IL}, V_{IH}, V_{OL}, V_{OH}, for CMOS inverter are taken as 0.33 V, 0.57 V, 0.06 V, 0.82 V respectively. Using these values the noise margins of CMOS inverter are calculated as:

$$NM_H = V_{OH}\text{-}V_{IH} = 0.82V - 0.57\ V = 0.25\ V$$
$$NM_L = V_{IL} - V_{OL} = 0.33\ V - 0.06\ V = 0.27\ V$$

Like CMOS inverter for carbon nanotube field effect transistor inverter also the values of the V_{IL}, V_{IH}, V_{OL}, V_{OH} are taken as 0.42 V, 0.48 V, 0.09 V, 0.81 V respectively. Using these values the noise margins of carbon nanotube field effect transistor inverter are calculated as:

$$NM_H = V_{OH}\text{-}V_{IH} = 0.81V - 0.48\ V = 0.33\ V$$
$$NM_L = V_{IL} - V_{OL} = 0.42\ V - 0.0.09\ V = 0.33\ V$$

An improved noise margin is thus observed in case of carbon nanotube field effect transistor. This improved VTC and hence noise margin is preserved even if the power supply voltage is decreased. A plot showing the VTC of carbon nanotube field effect transistor inverter and CMOS inverter at different power supply voltages is shown in Fig. 2(b).

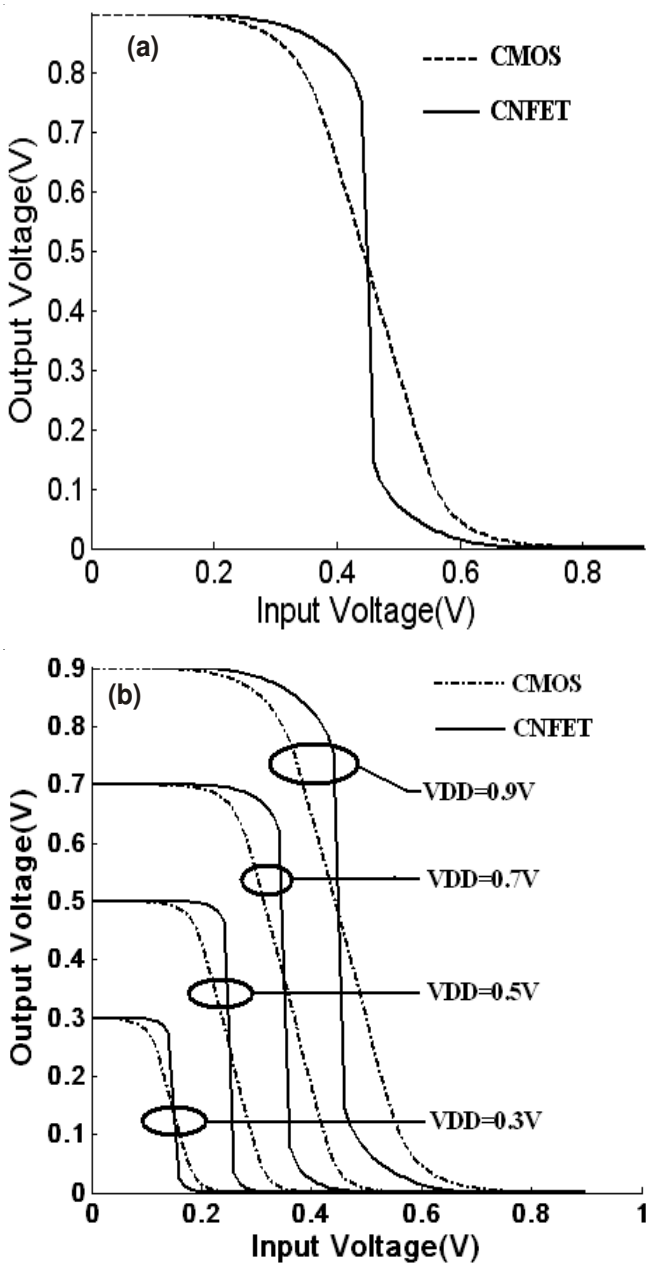

Fig. 2. Voltage transfer characteristics of CNFET inverter and CMOS inverter at (a) 0.9 V power supply; (b) different power supplies

The average power dissipation of both the carbon nanotube field effect transistor inverter and CMOS inverter is studied along with their corresponding delay times. It is found that carbon nanotube field effect transistor inverter shows improvement in both the cases as given in Table-1. Due to the presence of quasi 1D structure, offering ballistic carrier transport with negligible wide angle scattering rates, an improvement in delay of carbon nanotube field effect transistor inverter is observed in comparison to carbon nanotube field effect transistor inverter. Lower power dissipation of carbon nanotube field effect transistor inverter makes it an option for future low power applications. Fig. 3 shows that the inverter behaviour depends on the diameter of each nanotube affecting the delay of the inverter circuit. We can choose different diameter for optimization. But consi-dering the current fabrication conditions, minimum diameters are generally preferred.

TABLE-1
COMPARISON BETWEEN CNFET
INVERTER AND CMOS INVERTER

Key characteristics	CMOS inverter	CNFET inverter
Maximum Power (μW)	123.77	103.82
Average Power (μW)	2.40	2.11
Rise time Delay (ps)	24.06	21.0
Fall time Delay (ps)	30.40	21.0
Noise Margin (V)	$NM_H = 0.25$	$NM_H = 0.33$
	$M_L = 0.27$	$NM_L = 0.33$

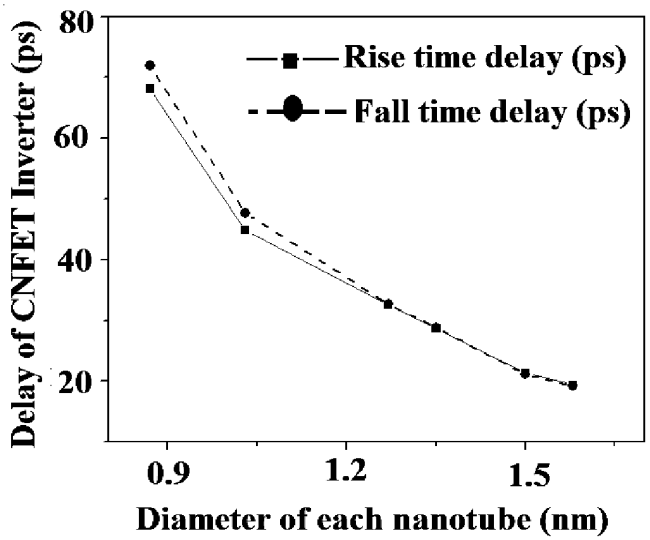

Fig. 3. Variation of rise time and fall time delay of CNFET inverter with diameter of each nanotube

Conclusion

Carbon nanotube field effect transistor device is now emerging as an excellent nanoscaled device that can overcome the limitations of scaled CMOS technology. In this paper we have simulated and analyzed the key performances of inverter like noise margin, average power and delay times. Further we have compared the simulation results of carbon nanotube field effect transistor inverter with that of the CMOS inverter. From this comparison we studied that for carbon nanotube field effect transistor inverter the average power consumption has reduced and an efficient improvement in noise margin is observed in comparison to CMOS inverter circuit. Significant improvements have been observed in rise and fall time delay. Finally it can be concluded that the improved performance of carbon nanotube field effect transistor inverter in comparison to CMOS inverter making it a better choice for future nano electronic circuits.

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