

Modeling and Performance Analysis of Graphene Field Effect Transistor†

S. BARDHAN* and H. RAHAMAN

School of VLSI Technology, Bengal Engineering and Science University, Shibpur, Howrah-711 102, India

*Corresponding author: E-mail: s.bardhan@rediffmail.com

AJC-12893

This paper presents a physics-based model and characteristics of drain current, field, velocity, electron density with variation of channel length of graphene and equivalent capacitive circuit model of field-effect transistors. Depending on drift-diffusion carrier transport and saturation velocity effects, the field effect transistor model has been designed. First, an explicit model has been derived for the drain current. These models have been simulated and the results obtained are in excellent agreement with the theoretical calculations.

Key Words: Field-effect transistor, Graphene, Modelling.

INTRODUCTION

Graphene is a single atomic layer of carbon atoms arranged into a two-dimensional (2D) hexagonal lattice. Since its discovery in 2004 by physicists¹ single layer graphene has been produced by many different methods and sample quality has steadily improved²⁻⁴. Despite being a semi-metal with zero energy gap, graphene differs from conventional metals in that its charge carrier density can be continuously tuned from *n*-type (*i.e.* carriers are electrons) to *p*-type (*i.e.* carriers are holes) simply by applying an electric field. The relation between the charge carrier energy *E* and the 2-D wave vector $k = \sqrt{k_x^2 + k_y^2}$ is linear, *i.e.*, $E = \pm \hbar v_F k$, where v_F ($\sim 10^8$ cm/s) is the Fermi velocity, thereby reducing the bandgap to a single point (Dirac point)⁵. In this framework, all carriers have a velocity with the same absolute value that is one order of magnitude larger than in conventional III-V materials⁶, making graphene a promising candidate for high-speed nanoelectronics. This is due to remarkable electronic properties like high mobility and saturation velocity together with a promising ability to scale to short gate lengths and high speeds by virtue of its thinness. Graphene field-effect transistors were successfully fabricated and exhibited I-V characteristics similar to conventional silicon MOS transistors⁷. An explicit compact model for the current-voltage (I-V) characteristics of graphene field-effect transistor was proposed⁸. Taking this work as a basis, which provides the DC behaviour. The physical framework is a field-effect model and drift-diffusion carrier transport with saturation velocity effects, which is accurate in explaining the characteristics

of drain current, field, velocity, electron density with variation of channel length of graphene.

THEORY

Computation of drain current: The source and drain are contacting the graphene channel and are assumed to be ohmic. The drain current model, which provides the basis for both charge and capacitance models⁸. The electrostatics of this device can be understood using the equivalent capacitive circuit depicted⁹ (Fig. 1). Here, C_t and C_b are the top and bottom oxide capacitances and C_q represents the quantum capacitance of graphene. The potential V_c represents the voltage drop across C_q and the relation between them is given by $C_q = k|V_c|$, where $k = [2q^2/\pi](q/(\hbar v_F)^2)$ and v_F ($= 10^6$ m/s) is the Fermi velocity. The overall net mobile sheet charge density in the graphene channel can be obtained:

$$V_c(x) = (V_{gs} - V_{gs0} - V(x)) \frac{C_t}{C_t + C_b + \frac{1}{2}C_q} + (V_{bs} - V_{bs0} - V(x)) \frac{C_b}{C_t + C_b + \frac{1}{2}C_q} \quad (1)$$

where $V_{gs} - V_{gs0}$ and $V_{bs} - V_{bs0}$ are the top and back gate-source voltage over drives, respectively. To model the drain current of the graphene field-effect transistor, a drift-diffusion transport is assumed under the form $I_{ds} = -W|Q_c(x)|v(x)$, where W is the gate width, $|Q_c|$ is the free carrier sheet density in the

†International Conference on Nanoscience & Nanotechnology, (ICONN 2013), 18-20 March 2013, SRM University, Kattankulathur, Chennai, India

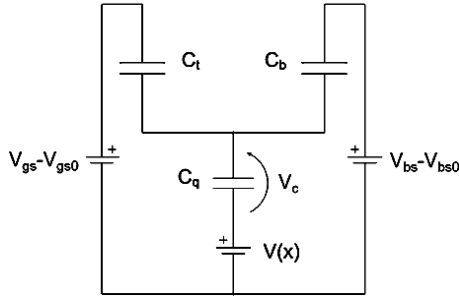


Fig. 1. Equivalent capacitive circuit of the dual-gate GFET

channel at position x and $v(x)$ is the carrier velocity and $v(x)$ can be expressed as:

$$v(E) = \frac{\mu E}{[1 + (\mu E / v_{\text{sat}})]} \quad (2)$$

where E is the electric field, μ is the carrier low-field mobility and v_{sat} is the saturation velocity. A more refined model, relating the saturation velocity with the carrier density, could be considered instead⁸. Applying $E = -dV(x)/dx$, combining the foregoing expressions for v and v_{sat} and integrating the resulting equation over the device length, the drain current becomes:

$$I_{\text{ds}} = \frac{\mu W \int_0^{V_{\text{ds}}} |Q_c| dV}{L + \mu \frac{|V_{\text{ds}}|}{v_F}} \quad (3)$$

The denominator represents an effective length L_{eff} that takes into account the saturation velocity effect. To get an explicit expression for the drain current, the integral in (3) is solved using V_c as the integration variable and consistently expressing Q_c as a function of V_c , *i.e.*,

$$I_{\text{ds}} = \frac{\mu W |Q_c(V_c)| \frac{dV}{dV_c} dV_c}{L + \mu \frac{|V_{\text{ds}}|}{v_F}} \quad (4)$$

Here, V_c is obtained from (1) and can be written as (5):

$$V_c = \frac{-(C_t + C_b) + \sqrt{(C_t + C_b)^2 \pm 2k[(V_{\text{gs}} - V_{\text{gs0}} - V)C_t + (V_{\text{bs}} - V_{\text{bs0}} - V)C_b]}}{\pm k} \quad (5)$$

where the positive (negative) sign applies when $(V_{\text{gs}} - V_{\text{gs0}} - V)C_t + (V_{\text{bs}} - V_{\text{bs0}} - V)C_b > 0$ (< 0). The channel potential at the source V_{cs} is determined as $V_c(V = 0)$. Similarly, the channel potential at the drain V_{cd} is determined as $V_c(V = V_{\text{ds}})$. Moreover, (1) provides the relation $dV/dV_c = -(1 + kV_c \text{sgn}(V_c)/(C_t + C_b))$ entering in (3), where sgn refers to the sign function. On the other hand, the charge sheet density can be written as $|Q_c(V_c)| = kV_c^2/2$. Inserting these expressions into (4), the following explicit drain current expression can finally be obtained:

$$I_{\text{ds}} = \frac{\mu k}{2} \frac{W}{L_{\text{eff}}} \{g(V_c)\}$$

$$g(V_c) = \frac{-V_c^3}{3} - \text{sgn}(V_c) \frac{kV_c^4}{4(C_t + C_b)} \quad (6)$$

$$L_{\text{eff}} = L + \mu \frac{|V_{\text{ds}}|}{v_F}$$

Explicit expression of graphene charge density: The total carrier density is determined by averaging charge balance and mass action relationship equation¹⁰ for the regions of $\pm \Delta$, which can be solved numerically but does not yield an explicit

expression. In order to simplify this, it is noted that at low charge density charge balance equation approaches unity. At large $|V_{\text{G0}}|$ the gate-induced charge dominates. Finally, we add a correction for the spatial charge inhomogeneity by noting that when this is taken into account the minimum carrier density n_0 . This results from averaging the regions of $\pm \Delta V_0$ near the Dirac point. Solving charge balance and mass action relationship equation with these approximations results in an explicit expression for the concentration of electrons and holes:

$$n, p \approx \frac{1}{2} \left[\pm n_{\text{cv}} + \sqrt{n_{\text{cv}}^2 + 4n_0^2} \right] \quad (7)$$

where n_{cv} carrier density including gate-induced and the lower (upper) sign corresponds to electrons (holes).

RESULTS AND DISCUSSION

The device under test has $L = 2 \mu\text{m}$, $6 \mu\text{m}$, $8 \mu\text{m}$ respectively and $W = 2.1 \mu\text{m}$, with top dielectric is of 26 nm and the bottom dielectric⁴ is silicon oxide of 285 nm. After simulation we have seen the characteristics are changing which shown in Figs. 2-4. The back-gate voltage was -40 V. The flat-band voltages V_{gs0} and V_{bs0} were tuned to 1.45 and 2.7 V, respectively. A low-field mobility of $1200 \text{ cm}^2/\text{V.s}$ for both electrons and holes, S/D resistance of 800Ω . These values are consistent with the extracted values. Sheet carrier density $\rho_0 = 10^{11} \text{ cm}^{-2}$ was selected for the final fine tuning.

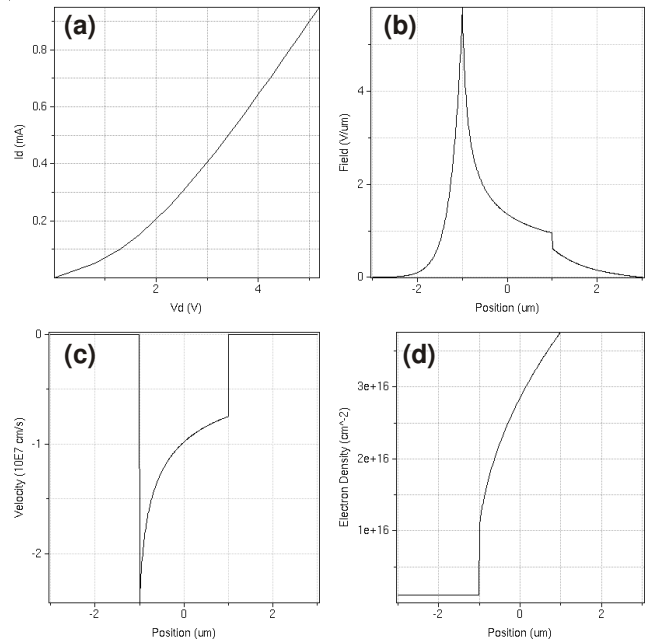
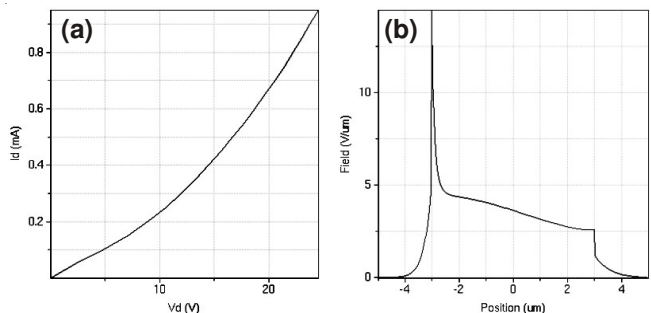


Fig. 2. (a) Drain current I_D versus drain voltage V_{ds} , (b) Field versus position, (c) Velocity versus position, (d) Electron density versus position for channel length $L = 2 \mu\text{m}$



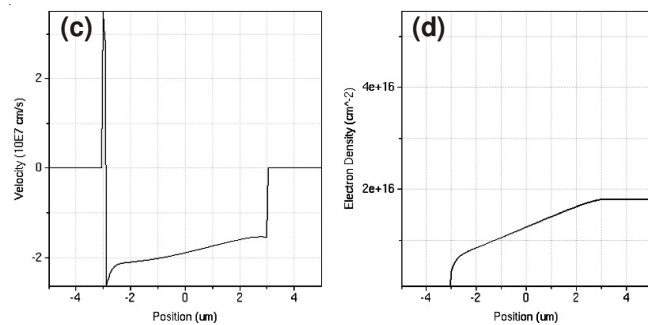


Fig. 3. (a) Drain current I_D versus drain voltage V_{DS} , (b) Field versus position, (c) Velocity versus position, (d) Electron density versus position for channel length $L = 6 \mu m$

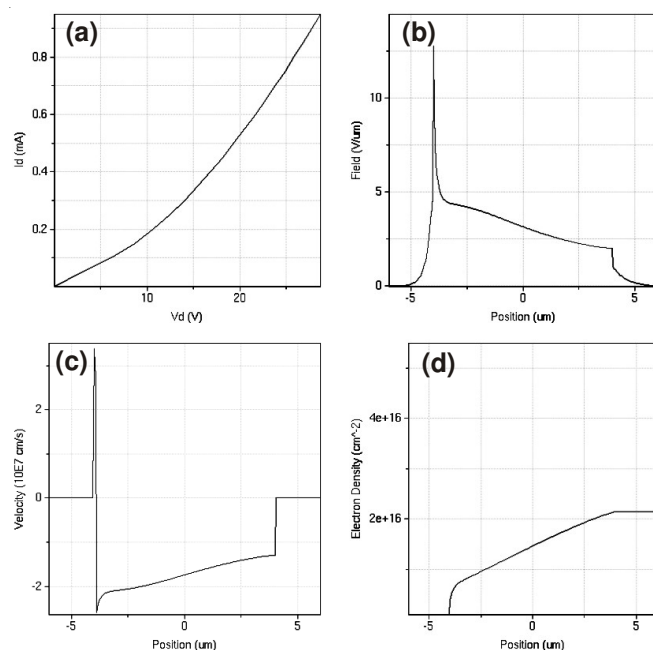


Fig. 4. (a) Drain current I_D versus drain voltage V_{DS} , (b) Field versus position, (c) Velocity versus position, (d) Electron density versus position for channel length $L = 8 \mu m$

Conclusion

This paper has presented a model for graphene field-effect transistors based on a field-effect model and drift-diffusion carrier transport, including saturation velocity effects. The model captures the physics of all operation regions within a single expression for the drain current and analysis the performance characteristics of drain current, field, velocity, electron density with variation of channel length of graphene.

REFERENCES

1. K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S.V. Dubonos, I.V. Grigorieva and A.A. Firsov, *Science*, **306**, 666 (2004).
2. C. Berger, Z.M. Song, T.B. Li, X.B. Li, A.Y. Ogbazghi, R. Feng, Z.T. Dai, A.N. Marchenkov, E.H. Conrad, P.N. First and W.A. de Heer, *J. Phys. Chem. B*, **108**, 19912 (2004).
3. Y. Zhang, J.P. Small, W.V. Pontius and P. Kim, *Appl. Phys. Lett.*, **86**, 073104 (2005).
4. X.L. Li, X.R. Wang, L. Zhang, S.W. Lee and H.J. Dai, *Science*, **309**, 1229 (2008).
5. A.K. Geim and K.S. Novoselov, *Nat. Mater.*, **6**, 183 (2007).
6. E. Kartheuser, Antwerp, Belgium: NATO Advanced Study Inst., pp. 717-7 (1971).
7. I. Meric, *Nat. Nanotechnol.*, **3**, 654 (2008).
8. D. Jiménez and O. Moldovan, *IEEE Trans. Electron Devices*, **58**, 4150 (2011).
9. S. Thiele, J.A. Schaefer and F. Schwierz, *J. Appl. Phys.*, **107**, 094505 (2010).
10. V.E. Dorgan, M.-H. Bae and E. Pop, *Appl. Phys. Lett.*, **97**, 082 (2010).