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# Surface-Modified Dielectric Materials for Transistor†

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Organic field-effect transistors operating at low voltage (< 2 V) have been fabricated using new solution-processable nanoscale dielectric as the gate dielectric material. In this paper, we demonstrate that a monolayer of octadecyltrichlorosilane on top of nanoscale dielectric shows good improved dielectric properties with optimized changing the surface characteristics and good insulating property with leakage current densities as low as $10^{-7}$ A/cm$^2$ at 1 V and capacitance value approaching 420 nF/cm$^2$. The corresponding pentacene transistors based on these dielectrics exhibit improved performance with hole mobility of ~ 0.2 cm$^2$/Vs and $I_{on}/I_{off}$ ratio ~ $10^5$.

**Key Words: Self-assembly, Dielectric, Transistor, Nanoscopic.**

## INTRODUCTION

Organic field-effect transistors are of interest in recent years for future organic electronics, such as RFID, flexible display and sensors[1]. Many *p*-type and *n*- type organic semiconductors are developed so far, but their intrinsic mobility are usually quiet low compare to inorganic semiconductors and need to apply high voltage to operate device[2]. Using this approach we can never develop portable device with battery. Several approaches have been proposed for reducing operating voltage[3]. At first, using reduced channel length can obtain the required drain current at low operating voltage because the drain current is inversely proportional to the channel length. However, this method needs expansive procedure such as e-beam lithography to pattern the channel to nanoscale. While the use of high-k materials such as $TiO_2$ as gate dielectrics is also another possible approach, but it is not compatible to plastic substrate for flexible display because we need very high temperature for this method. The promising method to low operating voltage is using very thin-film dielectric which provide high capacitance and low leakage current and it makes organic field-effect transistors to operate at lower than 2 V. Some groups make an effort to enable performance at very low operating voltage using SAMs and crosslinked polymer blend[4]. Nanoscale dielectric which are alternating layers of organic molecules inter connected by silane network[5]. Furthermore, nanoscale dielectric based devices show high capacitance and low leakage current and low interface trap states. However, for the organic semiconductor we just show the possibility for low operating voltage. The performance is relatively lower than device using regular silicon dioxide ($SiO_2$) layer for dielectrics. Here, we demonstrate high performance organic field-effect transistors with very low operating voltage using surface-modified nanoscale dielectric and air stable *p*-type semiconductors.

## EXPERIMENTAL

Pentacene was purchased from Aldrich and purified by gradient vacuum sublimation twice. Octadecyltrichloride silane (OTS) was purchased from Aldrich and used it without further purification. Octachlorotrisiloxane was purchased from Gelest. Prime grade silicon wafer were used as device substrate. Silicon wafers were cleaned by Piranha solution ($H_2SO_4$; 70 % and $H_2O_2$; 30 %) and were dried before using. All self-assembly procedures were performed in nitrogen atmosphere. The process of depositing NSD 1 and octadecyltrichloridesilane mulitilayers is shown in Fig. 1. The following procedure was carried out in a single-reaction vessel using standard cannula techniques. Pentacene were deposited under ultra-high vacuum ($3 \times 10^{-6}$ Torr) at the substrate temperature which kept in room temperature. AFM images were obtained from JEOL -5200 scanning probe microscopes in the tapping mode. For MIS structure, gold electrode (which area is 200 μm × 200 μm) were deposited by metal evapourating system and for FET structure, top contact electrodes were deposited through shadow mask with channel length and width defined as 100 μm

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and 1000 μm. All electrical measurements were performed with a Keithley 6430 sub-femtoamp remote source meter and a Keithley 2400 source meter using a locally written LABVIEW program and general purpose interface bus (GPIB) communication. Capacitance was measured on MIS structures using probe station with impedance analyzer (Hewlett-Packard 4192A). The device characterization was carried out under ambient conditions. The saturation mobility was calculated using the following equation, $I_{ds} = (W/2L)\cdot\mu\cdot C_i\cdot(V_G-V_{Th})^2$ where L is the channel length, W is the channel width, $C_i$ is the capacitance per unit area of the dielectric, μ is the field effect mobility of the semiconductor, V is the threshold voltage and $V_G$ is the gate voltage. The saturation mobility calculation was performed with linear section of plot of $I_{ds}^{1/2}$ *vs.* $V_G$ derived from the transfer plot of the device.

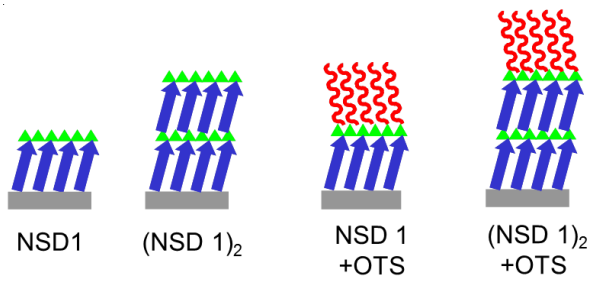


Fig. 1. Schematic illustration of our nanoscale dielectric

## RESULTS AND DISCUSSION

Schematic representation of our nanoscale dielectric and the molecular structure of nanoscale dielectric components are illustrated in Fig. 1. These nanoscale dielectric (NSD) are identified by the following nomenclature: i) NSD 1 (highly polarizable organic molecule + capping layer); ii) $[NSD\ 1]_2$ (double-layer of NSD 1); iii) NSD1 + OTS (OTS-treated NSD 1); iv) $[NSD\ 1]_2$ + OTS (OTS-treated $[NSD\ 1]_2$). We examined the leakage current and capacitance using the simplest dielectric film (NSD1). Pentacene FETs were fabricated by vapour-deposition of the semiconductor on top of NSD 1 dielectric followed by Au source and drain contact deposition. These organic field-effect transistors exhibit typical transistor characteristics when operated at lower voltage (< 2 V) although organic field-effect transistor based on conventional 300 nm thick $SiO_2$ dielectrics can operate at very high voltage (~100 V). However, the mobility (0.02 $cm^2$/Vs) and on/off ratio ($10^3$) of these organic field-effect transistors based on NSD 1 are lower than the devices fabricated on 300 nm thick $SiO_2$ (mobility ~0.3 $cm^2$/Vs and on/off ratio ~$10^5$). One of the reasons for the poor performance is the relatively large gate leakage current density (~$10^{-4}$ A/$cm^2$ at 1 V) of NSD 1. Another reason is associated with the relatively large surface roughness of NSD 1 films, which prevents optimal crystallization of the pentacene film. Indeed, atomic force microscope (AFM) images of pentacene films on top of NSD 1 indicate smaller crystallites than those found on smooth $SiO_2$. Correlation between pentacene film grain size and dielectric insulator surface morphologies are well known[6]. Root mean square (rms) roughness of the NSD 1 surface is 1~2 nm, much rougher than conventional Si-$SiO_2$ substrates (~0.1 nm), leading to small pentacene crystallites. Small pentacene grains afford more grain boundaries which prevent good charge transport. The combination of the large leakage current density and poor surface morphology of NSD 1 films prevents optimal organic field-effect transistor performance. Note that when pentacene is used as the semiconductor for FETs, greater performances are obtained on hydrophobic dielectrics (OTS-treated) instead of hydrophilic (bare $SiO_2$ substrates). However, since NSD 1 and $SiO_2$ surfaces are both highly hydrophilic, the substrate surface energy should not play a role in the different FET performance. In this paper, multilayer structures of NSD 1 are also investigated to analyze the effect of a reduced leakage current density. Furthermore, nanoscale dielectric films of NSD 1 capped with octadecyltrichloridesilane are fabricated to overcome the limitation of NSD 1 layers. The goals of these studies are to reduce leakage current density, vary surface morphology and change the surface chemistry of NSD 1 from hydrophilic to hydrophobic.

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Metal-insulator-semiconductor (MIS) structures were fabricated to measure the leakage current and capacitance of the new proposed nanoscale dielectric (Fig. 2). Compared to NSD 1 which shows current densities of $10^{-4}$ A/$cm^2$ at 1 V, $[NSD1]_2$,

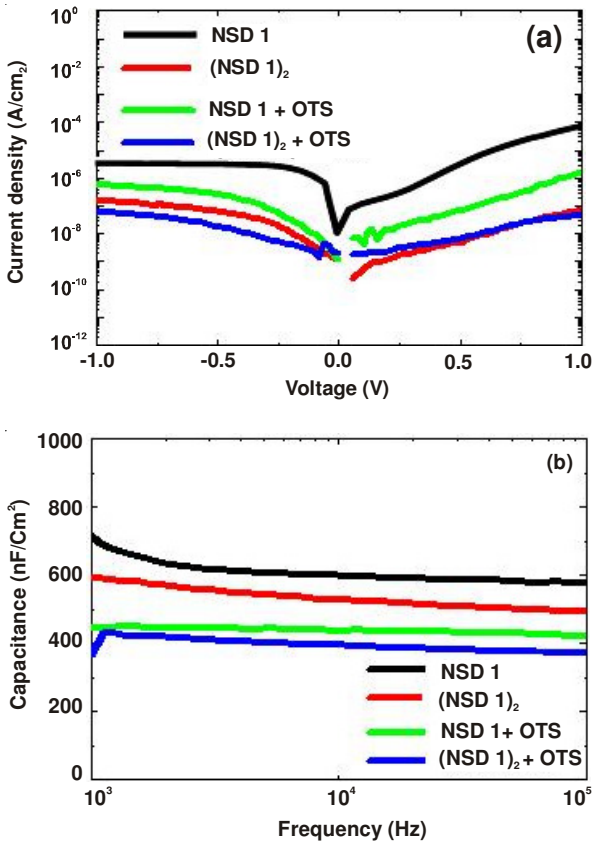


Fig. 2. (a) Measured leakage current density (*J*) *vs.* voltage (V) plots with nanoscale dielectric (NSD1, $[NSD1]_2$, NSD1 + OTS and $[NSD1]_2$ + OTS) in MIS sandwich structures on $n^+$-Si. (b) Capacitance *vs.* frequency (C-f) dependence of the capacitance in the accumulation regime (1 V) for each nanoscale dielectric in metal-insulator-semiconductor devices

NSD1 + OTS and $[NSD1]_2$ + OTS afford leakage current densities lower by 2-3 orders of magnitude for the same bias window. Capacitance-voltage (C-V) measurements were performed on the MIS structures and the capacitances are 600 nF/cm$^2$ (NSD 1), 510 nF/cm$^2$ ($[NSD\ 1]_2$), 420 nF/cm$^2$ (NSD 1 + OTS) and 390 nF/cm$^2$ ($[NSD1]_2$ + OTS) at 10 kHz. These values are much greater than the capacitance of 300 nm thick $SiO_2$ dielectrics (10 nF/cm$^2$). To characterize the dielectric surface morphology, we performed a detailed AFM analysis on the modified nanoscale dielectric films. The RMS roughness of NSD 1 (1.5 nm) could be reduced by OTS treatment to 1.0 nm (NSD 1 + OTS). Note that in the case of $[NSD\ 1]_2$ the RMS (2-3 nm) is larger than that of NSD1. Furthermore, upon OTS treatment, the contact angle of NSD1-OTS increases from 20º to 105º, rendering the substrate very hydrophobic. organic field-effect transistors are fabricated by depositing a 50 nm thick pentacene film by thermal evapouration on top of NSD1, $[NSD1]_2$, NSD1 + OTS and $[NSD1]_2$ + OTS dielectrics. Pentacene molecules strongly adhere on the hydrophobic surface due to the low surface energy. AFM was used to investigate the pentacene film morphology. The grain size of pentacene films is increased on OTS-treated substrate probably because of the lower surface energy and smoother dielectric surface (Fig. 3). X-ray diffraction was used to characterize the ordering of pentacene film on NSD 1 and

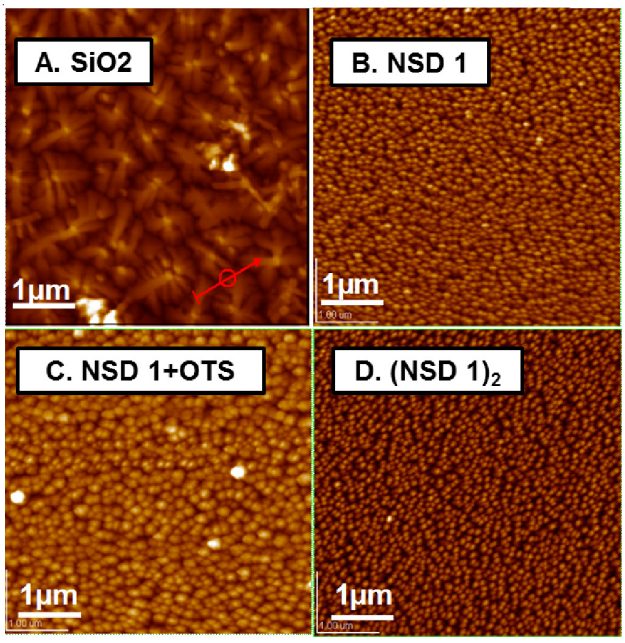


Fig. 3. Tapping mode AFM images (5 × 5 µm scan area) for morphology evaluation of 50 nm pentacene film grown at room temperature on the each nanoscale dielectric substrates. (A. 300 nm thick $SiO_2$, B. NSD1, C. NSD 1 + OTS, D. $[NSD1]_2$)

NSD1+OTS dielectrics (Fig. 4). The intensity of the XRD reflections is increased after OTS treatment, indicating ordering of pentacene is also affected by the hydrophobic dielectric surface[7]. Organic field-effect transistors (channel length 100 µm and channel width 1000 µm) were completed by thermal deposition of Au and the electrical properties were tested (Table-1). Fig. 5 shows the representative transfer plots for pentacene organic field-effect transistors based on NSD1, $[NSD1]_2$, NSD1 + OTS and $[NSD\ 1]_2$ + OTS. From these data, the average field-effect mobility is calculated in the saturation regime ($V_G < V_{DS} = -2$ V) by plotting the square root of the drain current *versus* gate voltage. The field effect mobility is 0.02 cm$^2$/Vs for NSD1-based device and increases to only 0.04 cm$^2$/Vs for the double-layer $[(NSD\ 1)_2]$ dielectrics although the leakage is reduced by 100 × compared to NSD1. However, the mobility dramatically increased to 0.2 cm$^2$/Vs for the OTS-treated dielectrics. This improvement is clearly due to a reduction of dielectric surface energy coupled with the improved ordering of pentacene molecules on the OTS treated dielectric surface.

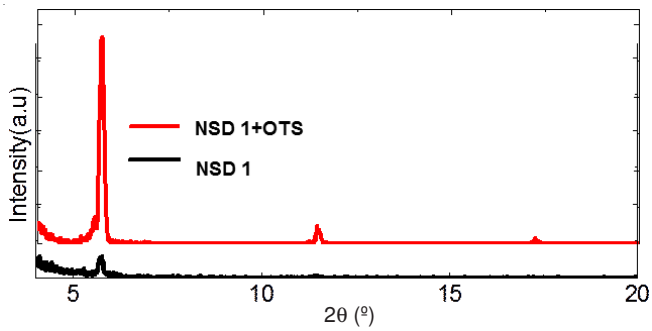


Fig. 4. Representative X-ray diffraction patterns of a 50 nm pentacene film deposited on : a) NSD 1 nanoscopic dielectric and b) NSD 1+OTS nanoscopic dielectric. The peak correspond to d = 15.5 Å

TABLE-1
PROPERTIES OF EACH DIELECTRICS AND CHARACTERISTICS OF PENTACENE OFETs WITH THE DIELECTRICS AS GATE INSULATOR. ROOT MEAN SQUARE VALUE (rms) AND CONTACT ANGLE OF EACH DIELECTRICS

| Nanoscale dielectric (NSD) | | | | Pentacene FET parameters | | |
|---|---|---|---|---|---|---|
| Name | Capacitance (nF/cm$^2$) | rms (nm) | $\theta_{CA}$ (º) | $\mu_{sat}$ | $I_{on}$:$I_{off}$ | $V_T$ |
| NSD1 | 600 | 1.5 ± 0.5 | 20 | 0.02 | $10^3$ | -0.7 |
| $(NSD1)_2$ | 510 | 2.5 ± 1.0 | 20 | 0.04 | $10^4$ | -0.6 |
| NSD 1 + OTS | 420 | 1.0 ± 0.3 | 105 | 0.20 | $10^5$ | -0.7 |
| $(NSD1)_2$ + OTS | 390 | 2.3 ± 1.0 | 105 | 0.15 | $10^5$ | -0.6 |

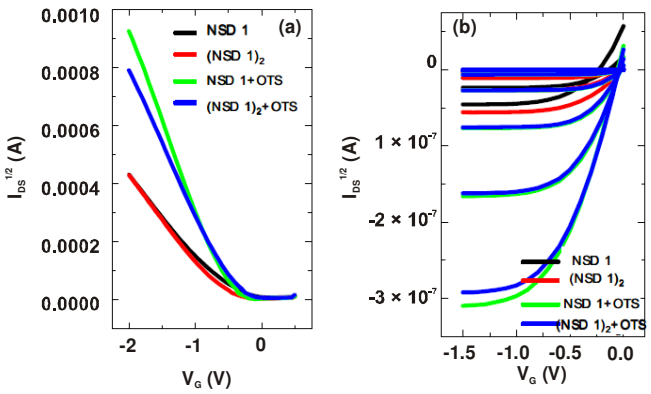


Fig. 5. Representative pentacene FET device performance at low bias with each nanoscale dielectric on n$^+$-silicon gate (L/W = 100/1000 µm). (a) FET transfer plot of $[I_{SD}]^{1/2}$ *vs.* $V_G$ at $V_{SD}$ = -2 V.B. Current-voltage output plot as a function of $V_G$ at $V_{SD}$ = -1.5 V

## Conclusion

High capacitance and low leakage current of the surface-treated nanoscale dielectric using self-assembled monolayer (SAM) has been demonstrated. These dielectrics can be used for low-operating-voltage pentacene organic field-effect transistor devices.

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