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Leakage Current Through the Ultra Thin Silicon Dioxide

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A significant issue *i.e.*, leakage of current through the gate oxide, has been considered relevant to the use of ultra thin (< 1-2 nm) pure oxides of silicon in the next complementary metal oxide semiconductor (CMOS) device generation based on the analytical Landauer-Buttiker method. The ratio of leakage of current through the single and double oxide was also estimated. The result shows that the double gate can reduce the leakage of current.

Key Words: Thin film, Nano transistor, CMOS, Gate oxide dielectric, Landaure-Buttiker method.

INTRODUCTION

Silicon oxide has received a tremendous attention in the last 40-50 years. It has been an excellent gate dielectric of complementary metal oxide semiconductor (CMOS) devices. Due to it's good structure and amorphous interface between it and silicon substrate and the other properties quoted[1-4] numerous attempts to find a viable gate dielectric for CMOS have encountered two major difficulties: (1) increasing leakage current and (2) born penetration from poly silicon gate electrode through ultra thin silicon oxide. Indeed a further reduction of gate oxide thickness produces an exponential increase of direct tunneling leakage current posing a fundamental limit for further scaling[5]. However, to date, no other gate dielectric could replace to silicon oxide and fill this gap.

Some researchers have suggested several high-k dielectrics for replacement of SiO_2[6]. To overcome this scaling limit of silicon oxide as gate insulator. But, these materials can affect the carrier mobility through the channel of transistors. In this work, we have studied the quantized conductance of a ballistic quantum wire (QWR) from contact resistances and disturbing the current flow. By using the direct transmission probability of each probe contact and Landaure-Buttiker formalism, a solution to overcome the scaling limit of silicon oxide as gate dielectric is it's substitution by double gate insulator. Because double gate can reduce the leakage current then single gate and thus appear to be promising candidate for future CMOS generations.

Theory: Referring to previous work[7] and the current literature[8], the future of CMOS integration requires improvements of the gate dielectric materials. In this

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work, we used sample geometry in Fig. 1, for four terminals resistance measurements on a QWR with Ohmic contact in interface between electrode and channel. With such geometries, the QWR in particularity quantum point contacts (QPCs) is produces by tuning the gate voltage to negative values, such that the electron gas underneath gets depleted.

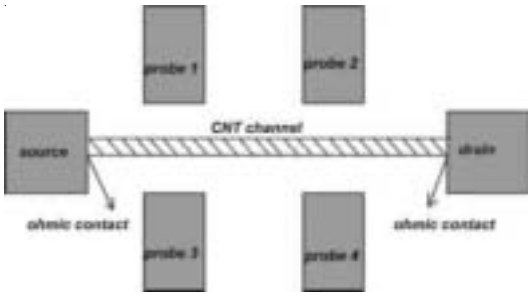

Fig. 1. Sample geometry with 4 voltage probe

In this regime a further reduction of the gate voltage, cause the lateral electric field and with it the lateral depletion zone around the gates increases, we can thus tune the electronic width and change the number (j) of occupied modes of the QPC. In a simple picture, one can imagine that at the absence of magnetic fields, the fraction of the electron trajectories close to the wire edge is minimized and the conductance of such QPCs can be quantized in units of j2e2/h. In this picture, the QPCs is connected to source S and drain D *via* a transition region by ballistic, strictly one-dimensional QWRs and the QPC itself by a barrier with transmission probability T, as shown in Fig. 2.

Fig. 2. A QPC as a transition region between source and drain (left) and it's idealized mode (right). This region is one-dimensional lead and the constriction is a barrier with transmission probability T

EXPERIMENTAL

The Silicon samples (n-type, 5 Ω cm, 1 cm × 1 cm) were cut out of wafers with 2 mm thickness. These samples were introduced in quartz tube. The schematic of sample layout in Fig. 3, clearly shows that one gate can be active gate (*e.g.* 2), while two other gates grounded. In this case, the operation mode around gate 2, *i.e.* the

left and right of gate 2 serve as source and drain. Now, let us show a top view of ballistic quantum wires circuit (Fig. 3). The gate is poly silicon and gate dielectric is the ultra thin silicon oxide. It is assumed that each contact can absorb all incoming electrons and distribute the emitted electrons equally among all out going model in which it can be filled up to the electrochemical potential of this contact (μ) at zero temperature. We define $T_{q\leftarrow p} = T_{qp} > 1 (T_{q\leftarrow p} = T_{qp})$ as a direct transmission probability of contact p (q) into contact q (p). Therefore, the data of reference[9] and the current conservation law, we can apply the Landaure-Buttiker formula as follow:

$$I_p = \sum_{q \neq p} \left(T_{q\leftarrow p} \mu_p - T_{p\leftarrow q} \mu_q \right) \tag{1}$$

To the sample shown in Fig. 3 and or

$$I_P = \sum_{q} G_{p\leftarrow q} \left(V_p - V_q \right) \tag{2}$$

where

$$G_{p\leftarrow q} = \frac{2e}{h} T_{p\leftarrow q} \text{ and } V_q = \frac{\mu_q}{e} \tag{3}$$

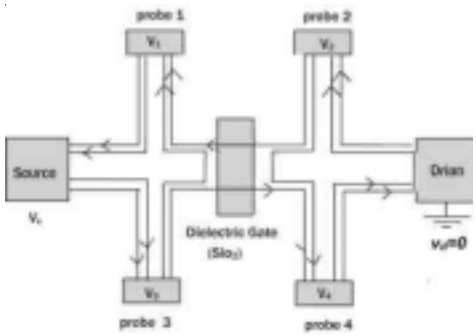

Fig. 3. Edge states in system with 4 voltage probe

RESULTS AND DISCUSSION

It is believed[10] that there is a negative oxide can silicon substrate and incoming oxygen should penetrate through the oxide film. To make bond with silicon atoms at the interface likewise, the electrons here can percolate all the way to the opposite edge, as shown in Fig. 3. From the work of Buttiker[11], a gate stripe extend across this region and changes the number of occupied landau levels that measured with 4 voltage probes. By tuning biasing the gate the electron density we can arrive at the point that the filling factor under the gate will be smaller than outside the gated area. Then edge states will get redirected at the gate. Now, we denote N and M for filling factor in the ungated and gated region, respectively based on the Landaure-Buttiker rule, we have

$$\begin{bmatrix} I_S \\ I_D \\ I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = G \begin{bmatrix} N & 0 & 0 & 0 & -N & 0 \\ 0 & N & 0 & -N & 0 & 0 \\ N & 0 & N & 0 & 0 & 0 \\ 0 & 0 & -N & M & N-M & 0 \\ 0 & 0 & 0 & N-M & M & -N \\ 0 & -N & 0 & 0 & 0 & N \end{bmatrix} \begin{bmatrix} V_s \\ V_D \\ V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \quad (4)$$

which yields to

$$V_1 = V_s,\ V_2 = \frac{I}{NG}, V_3 = \left(\frac{M-N}{M}\right)\frac{I}{NG},$$
$$V_4 = 0, V_s = \left(\frac{2M-N}{M}\right)\frac{I}{NG} \quad (5)$$

$$R_{12} = \frac{M-N}{M}\frac{1}{NG}$$
$$R_{13} = \frac{1}{NG}, R_{14} = \frac{2M-N}{M}\frac{1}{NG} \quad (6)$$
$$R_{24} = \frac{1}{NG}, R_{23} = \frac{1}{MG}$$

where $G = 2e^2/h$.

The main point is that the edge states (and or carriers) can not be redirected completely at the gate. Some carriers can pass through the gate for ultra thin gate oxide below 1-2 nm, this leakage current (labeled by factor of s) is of importance and the above obtained results should be modified as follow:

$$\begin{bmatrix} I_S \\ I_D \\ I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = G \begin{bmatrix} N & 0 & 0 & 0 & -N & 0 \\ 0 & N & 0 & -N & 0 & 0 \\ -N & 0 & N & 0 & 0 & 0 \\ 0 & 0 & -N & M & N-(M+S) & 0 \\ 0 & 0 & 0 & N-(M+S) & M & -N \\ 0 & -N & 0 & 0 & 0 & N \end{bmatrix} \begin{bmatrix} V_s \\ V_D \\ V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \quad (7)$$

So

$$V_1 = V_s,\ V_2 = \frac{I}{NG}, V_3 = \left(\frac{M+S-N}{M}\right)\frac{I}{NG},$$
$$V_4 = 0, V_s = \left(\frac{2M+S-N}{M}\right)\frac{I}{NG} \quad (8)$$

$$
\begin{aligned}
R_{12} &= \frac{2(M-N)+S}{M}\frac{1}{NG} \\
R_{13} &= \frac{1}{NG}, R_{14} = \frac{2M+S-N}{M}\frac{1}{NG} \\
R_{24} &= \frac{1}{NG}, R_{23} = \frac{S+N}{MNG}
\end{aligned}
\tag{9}
$$

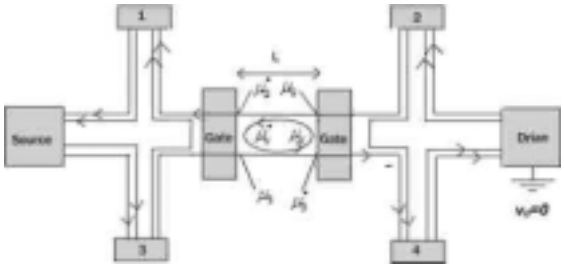

Fig. 4. Sample geometry with double gate oxide

If we consider a double gate dielectric as shown in Fig. 4 and solved the Landaure-Buttiker equation for such this system, we then have:

$$
\begin{aligned}
&V_1 = V_s,\ V_2 = \frac{I}{NG}, V^*_3 = \left(\frac{M-N}{M}\right)\frac{I}{NG}, \\
&V_4 = 0, V_s = \left(\frac{2M-N}{M}\right)\frac{I}{NG}, V_3 = -\frac{I}{NG} \\
&V_2^* = \frac{3MN-N^2-M^2}{M^2N}\frac{I}{G}, V_C = \frac{V_3 - V_3^*}{2}
\end{aligned}
\tag{10}
$$

$$
\begin{aligned}
R_{12} &= \frac{(M-N)}{M}\frac{1}{NG} \\
R_{13} &= \frac{3M-N}{NG}, R_{14} = \frac{2M-N}{M}\frac{1}{NG} \\
R_{24} &= \frac{1}{NG}, R_{23} = \frac{2}{NG}
\end{aligned}
\tag{11}
$$

which is a consequence of charge conservatise and with $\mu C = -*\mu_C$, $\mu_d = 0$.

The comparison of single and double gate dielectric results that mentioned above, the carriers penetration through the double gate is lower than that for a single gate dielectric, because the carriers encountered to two barriers in double gate.

Conclusion

In this work, the double oxide gate dielectric has been investigated in detail with the Landaure-Buttiker equation. Double oxide gate can reduce leakage of current more than that single oxide gate. We thus suggest double gate oxide to replace single gate dielectric for the future of CMOS generations[10-18].

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